OIP CS-03-016

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March 19, 2004

o: Commissioner for Patents P.O.Box 1450

Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572

28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/767,292 01/29/04

Hai Cong et al.

A NOVEL METHOD TO CONTROL DUAL DAMASCENE TRENCH ETCH PROFILE AND TRENCH DEPTH UNIFORMITY

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

CS-03-016

- U.S. Patent 6,603,204 to Gates et al., "Low-K Interconnect Structure Comprised of a Multilayer of Spin-on Porous Dielectrics," describes a two layer hard mask structure.
- U.S. Patent 6,309,962 to Chen et al., "Film Stack and Etching Sequence for Dual Damascene," teaches that two or three layers of hard mask are not needed in this process using an etch stop layer.
- U.S. Patent 6,605,874 to Leu et al., "Method of Making Semiconductor Device Using an Interconnect," discloses a multiple hard mask layer process with no etch stop layer.
- U.S. Patent 6,472,306 to Lee et al., "Method of Forming a Dual Damascene Opening Using CVD Low-K Material and Spin-on-Polymer," describes a single hard mask layer and not etch stop layer.

Sincerely,

Stephen B. Ackerman,

Req. No. 37761

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